



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,460	09/10/2003	Myounggoo Lee	101136-00095	2221

7590 05/02/2005

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 400
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER

VERSTEEG, STEVEN H

ART UNIT	PAPER NUMBER
----------	--------------

1753

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/658,460

Applicant(s)

LEE ET AL.

Examiner

Steven H. VerSteeg

Art Unit

1753

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/10/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the abstract is greater than 1 paragraph long and is greater than 150 words long. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3, and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,725,739 to Hu.
5. For claim 1, Applicant requires a bias sputtering film forming process for forming a thin film by applying both voltages of a cathode voltage and a substrate bias voltage, wherein a thin film is formed on a substrate whereon an irregularity is formed in the state wherein only the cathode voltage out of said both voltages applied, and sputtering film forming is performed while

Art Unit: 1753

varying said substrate bias voltage so that the thickness of said thin film formed on the surfaces on the sidewalls and on the bottoms of said irregularity is substantially uniform.

6. Hu discloses a process of forming a film in a recess of a substrate (abstract) comprising applying a DC bias to a target and no bias to a substrate in a first phase to deposit an overhang portion at the top of the recess (col. 6, l. 10-37). Thereafter, a resputter scheme is started in which the bias to the target is initiated and the material is redistributed so that the material is uniform (col. 6, l. 38-55). The bias to the substrate is varied because it is initially off and then is on.

7. For claim 3, Applicant requires the sputtering particles to be substantially vertically entering the substrate. The materials during resputtering are vertical because they are at a 0 degree angle (col. 7, l. 2-3).

8. For claim 5, Applicant requires a bias sputtering film forming apparatus comprising an AC power source of a DC power source of variable output against substrate electrodes and a control system wherein the control system makes the cathode voltage set to a predetermined voltage previously, stores the substrate bias voltage value when the substrate is apart from the target by a predetermined distance and the thickness distribution of thin films on each of said surfaces corresponding to said substrate bias voltage value as reference data, and controls the output of said power source by bias voltage functions produced by selecting the substrate bias voltage value that makes said film thickness substantially uniform from said reference data when each of said surfaces is formed.

Art Unit: 1753

9. As noted above, Hu discloses providing a DC power to the target and a DC power to the substrate (col. 6, l. 10-20) and inherently has some sort of control system based upon the fact that all of the biases are controlled.

10. Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,193,855 B1 to Gopalraja et al. (Gopalraja).

11. Claims 1, 3, and 5 are described above. For claim 2, Applicant requires the cathode voltage to be varied while varying the substrate bias voltage.

12. Gopalraja discloses a sputtering process whereby a DC bias is supplied to the target and a DC bias is supplied to the substrate (col. 5, l. 2-6). The sputtering involves filling a substrate via (Figures 1 and 2). There are two phases to the sputtering. In the first phase, bias is supplied to the target and no bias is supplied to the substrate (col. 7, l. 34-42). In the second phase, the target bias is terminated (col. 8, l. 24-26) and a variable bias is applied to the substrate (Figure 6). In the first phase, more material is deposited on the sidewalls than on the bottom of the via (col. 7, l. 44-48) and thus, an irregularity is present. As can be seen From Figures 5 and 6, the bias to the substrate and target are varied. During the second phase, the sputtered particles are substantially vertical (col. 8, l. 26-44). The substrate bias and target bias are controlled by a controller (Figure 3).

13. For claim 6, Applicant requires the apparatus further comprises a power source of variable output against said cathode, wherein said control system also varies the cathode voltage by controlling the output of said cathode power source, said bias sputtering film forming performed by controlling the output of said substrate power source based on said bias voltage functions.

Art Unit: 1753

14. Gopalraja discloses the power source to be variable to the target and substrate (Figures 5 and 6) and to be controlled by a controller (Figure 3).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,193,855 B1 to Gopalraja et al. (Gopalraja) in view of US 2002/0173144 A1 to Yamamoto.

17. For claim 4, Applicant requires the thin film to be used as a barrier layer or a seed layer for electrolytic plating.

18. Gopalraja is described above, but does not disclose what the deposited layer would be for. The disclosure is merely a teaching of how to adequately deposit a layer in a via of a substrate.

19. Yamamoto discloses that to when making a semiconductor integrated circuit, it is conventional to fill the recessed portion of the trench or via with a metal film such as copper by electrolytic plating after a copper seed layer is deposited by sputtering [0007]. When depositing the seed layer, it is conventionally to use a substrate bias to improve the substrate coverage [0012].

20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Gopalraja to deposit the layer in a via as a seed layer of copper and then fill it electrolytically because of the desire to form a semiconductor device.

Art Unit: 1753

21. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,725,739 to Hu in view of US 2002/0173144 A1 to Yamamoto.

22. Claim 4, Hu, and Yamamoto are described above. Hu does not disclose what the deposited layer would be for.

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Hu to deposit the layer in a via as a seed layer of copper and then fill it electrolytically because of the desire to form a semiconductor device.

General Information

For general status inquiries on applications not having received a first action on the merits, please contact the Technology Center 1700 receptionist at (571) 272-1700.

For inquiries involving Recovery of lost papers & cases, sending out missing papers, resetting shortened statutory periods, or for restarting the shortened statutory period for response, please contact Denis Boyd at (571) 272-0992.

For general inquiries such as fees, hours of operation, and employee location, please contact the Technology Center 1700 receptionist at (571) 272-1300.

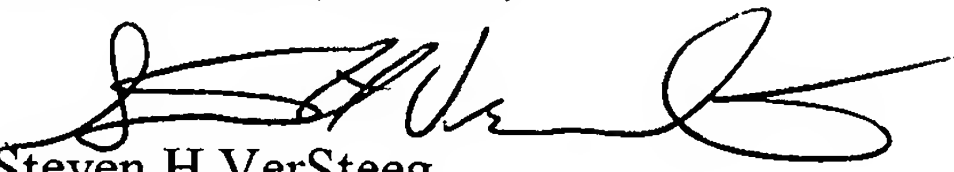
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. VerSteeg whose telephone number is (571) 272-1348. The examiner can normally be reached on Mon - Thurs (6:30 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 1753

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven H VerSteeg
Primary Examiner
Art Unit 1753

shv
April 28, 2005